Abstract of the Disclosure

Complementary bipolar transistors are fabricated on a semiconductor wafer by forming, on an upper surface of the semiconductor wafer, a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor. A first impurity is selectively introduced into the first and second electrodes. Then, a third electrode corresponding to the first transistor if formed, the third electrode being self-aligned with and electrically isolated from the first electrode, and a fourth electrode is formed corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode. A second impurity is selectively introduced into the third and fourth electrodes. A first active region of the first transistor and a first active region of the second transistor are formed, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors. Likewise, a second active region of the first transistor and a second active region of the second transistor are formed, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors. A reduction in the number of fabrication steps and/or masks is thereby achieved which reduces an overall cost of fabricating complementary bipolar transistors.